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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,487	11/03/2000	Jean-Didier Allegrucci	003242.P015	7643

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EXAMINER	
THAI, XUAN MARIAN	
ART UNIT	**PAPER NUMBER**
2111	7

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/705,487	ALLEGRUCCI, JEAN-DIDIER	
	Examiner	Art Unit	
	XUAN M. THAI	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/10/03*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1. This is in response to Amendment filed on November 10, 2003. Claims 1-2, 6-8, 12-14, and 18 have been amended. Claims 19-21 have been added. Claims 1-21 are now pending in the instant application.

2. The rejection of claims 2, 8 and 14 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, have been obviated by the amendment to those claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Jones et al. (USPN 6,356,960; Jones).

5. As per claims 1-2 and 7-8, Jones discloses the claimed invention including a method comprising: recognizing an occurrence of a user-specified event (recognizing control signals being transmitted by external debugging device; see Abstract or CPU executing an "event" instruction or decode special "event"; col. 8, lines 26-67; col. 9, lines 1-15; col. 11, lines 40-67); generating a signal to cease bus access (issuing instructions to cease fetching and enter the suspend state; col. 9, lines 15-26; col. 12, lines 12-18) in a configurable system on a chip (computer system on integrated chip; Abstract), upon the occurrence of the user-specified event, the configurable system on a chip integrating at least a central processing unit (CPU0 12 and 13), an internal system bus (e.g. p-link 15 or pipeline) and a configurable logic (e.g. event logic 44); allowing completion of all pending bus transactions (causes a CPU to drain the execution pipelines; col. 9, lines 35-38; col. 10, lines 15-18); stopping the system clock (stops all CPU execution or CPU is suspended; col. 9, lines 23-26) such that the state of the hardware is held static (see col. 9, lines 50-56); and accessing the static state of the hardware through a debug port (debug port 30) [see col. 9, lines 50-55].

As per claims 3 and 9, wherein the debug port is a bus master would be within the teachings of Jones in that Jones discloses external debugging device is operable to transmit control signals through the debugging port to stop CPU execution; to load a debugging routine to be executed by the CPU; and to restart operation of the CPU. Essentially, the external debugging device masters over the p-link bus through the debugging port to perform the above stated functions. Therefore, the debug port can be seen as a bus master (Abstract).

As per claims 4 and 10, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions (e.g. col. 9, lines 35-38).

As per claims 5 and 11, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions (e.g. col. 9, lines 35-38).

As per claims 6 and 12, wherein the specified event is programmed by a user (e.g. col. 12, lines 47-58).

As per claims 13 and 14, Jones discloses the claimed invention including an apparatus comprising: means (event logic 44) to recognize an occurrence of a user-specified event (col. 8, lines 26-67; col. 9, lines 1-15; col. 11, lines 40-67); means (event logic 44; prefetcher 101 and despatcher 103) to cease bus access (col. 9, lines 15-26; col. 12, lines 12-18) in a configurable system on a chip (computer system on integrated chip; Abstract), upon the occurrence of the user-specified event, the configurable system on a chip integrating at least a central processing unit (CPU0 12 and 13), an internal system bus (e.g. p-link 15 or pipeline) and a configurable logic (e.g. event logic 44); means to allow completion of all pending bus transactions (e.g. including event logic 44 causes a CPU to drain the execution pipelines; col. 9, lines 35-38; col. 10, lines 15-18); means to stop the system clock (e.g. including event logic 44, stops all CPU execution or CPU is suspended; col. 9, lines 23-26) such that the state of the hardware is held static (see col. 9, lines 50-56); and means to access the static state of the hardware through a debug port (debug port 30) [e.g. including external debugging device; see col. 9, lines 50-55].

As per claim 15, wherein the debug port is a bus master would be within the teachings of Jones in that Jones discloses external debugging device is operable to transmit control signals

through the debugging port to stop CPU execution; to load a debugging routine to be executed by the CPU; and to restart operation of the CPU. Essentially, the external debugging device masters over the p-link bus through the debugging port to perform the above stated functions. Therefore, the debug port can be seen as a bus master (Abstract).

As per claim 16, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions (e.g. col. 9, lines 35-38).

As per claim 17, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions (e.g. col. 9, lines 35-38).

As per claim 18, wherein the specified event is programmed by a user (e.g. col. 12, lines 47-58).

As per claims 19-21, wherein the user-specified event comprises a sequence of events (e.g. see cols. 9-12).

Response to Arguments

6. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

XUAN M. THAI
Primary Examiner
Art Unit 2111

XMT